A-1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,133	12/09/2003	Gee Sung Chae	053785-5053-01	3202

9629 7590 02/09/2005

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,133	CHAE ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-21 and 34-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-21 and 34-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/133,320.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/9/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims

Claims 13-21 and 34-42 are pending. Claims 1-12 and 22-33 have been cancelled per Preliminary Amendment of December 9, 2003.

Priority

Priority to Korean Patent Application No. 2001-58961 (Sept. 24, 2001) is claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13-16, 20-21, 34-37 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States patent 5,995,177 (to Fujikawa et al.) in view of United States Patent 6,091,473 (to Hebiguchi) and further in view of United States Patent 6,587,162 B1 (to Kaneko et al.).

As to claim 13: Fujikawa has, referring to Figure 9, a transparent insulative plate (substrate)(item 101), a second transparent substrate facing the (first) transparent insulative plate (not shown), a plurality of gate signal lines (102) arranged on the transparent substrate (101) along a first direction, source signal lines (data lines) arranged along a second direction perpendicular to the first upon a gate insulation layer (please see Figure 9) and defining pixel regions as can be seen in Figure 9, thin film transistors (not enumerated) connected to both gate and source signal lines and where the TFTs are formed in pixel regions, storage capacitance common lines (103) arranged in a vertical direction adjacent to the gate lines (102)(please refer to Figure 10).

Fujikawa also has a pixel electrode (5) formed on the insulative layer (18) and contacting the storage capacitor electrode (Figure 4) through the first contact hole, 11, – Figure 4). Pixel regions are defined as illustrated in Figure 3 (claims 11 and 12).

Fujikawa does not appear to explicitly specify that the storage capacitance common line has a protrusion and a first capacitor electrode overlaps a portion of the common line and protrusion of the common line to form a first storage capacitor, the first capacitor electrode connected to the thin film transistor.

Hebiguchi teaches and discloses an active matrix liquid crystal display wherein, with reference to Figure 1A, a common electrode wiring line (55) has common electrodes (53)

extending from the common electrode wiring line. A capacity generating electrode (65) overlaps the common electrode (bottom left hand corner of Figure 1A) and the capacity generating electrode (65) is connected to the drain electrode (63). Hebiguchi has this structure so that capacity is secured and capacity generated by the capacity generating electrodes functions as the removal of the effect of parasitic capacity when liquid crystal is driven and storage capacity for holding signal voltage (Column 6, Lines 30-49).

Hebiguchi is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to overlap a capacity generating electrode with a common electrode protruding from a common electrode wiring line and connecting the capacity generating electrode and drain for secured capacity and for removal of the effect of parasitic capacity when liquid crystal is driven and storage capacity for holding signal voltage.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Fujikawa in view of Hebiguchi for an array substrate in which capacity is secured, the effects of parasitic capacity are removed, and for storage capacity for holding signal voltage.

Fujikawa does not appear to explicitly specify a black matrix on the second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and the common line and a common electrode on the second transparent substrate to cover the black matrix.

Kaneko teaches and discloses a liquid crystal display wherein a black matrix is formed on an opposing substrate and shields portions of a gate line and drain line and furthermore shields a common line (Column 3, Lines 60-65 and Column 4, Lines 9-12). Kaneko also teaches that

typically a black matrix is formed on an upper color filter substrate and has a common electrode layer over a black matrix (Column 1, Lines 46-49).

Such a configuration of the black matrix with respect to the gate line and common line contributes to improved yield by preventing disconnection from occurring in a layered line portion or lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12).

Kaneko is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to specify a black matrix on the second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and the common line and a common electrode on the second transparent substrate to cover the black matrix for improved yield by preventing disconnection from occurring in a layered line portion or lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12).

Therefore at would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Fujikawa in view of Kaneko for improved yield by preventing disconnection from occurring in a layered line portion or lead terminal portion of an active matrix liquid crystal display device (Column 1, Lines 5-12).

As to claims 14 and 15, it may be presumed that the storage capacitance common line and gate line are of the same material (claim 14) for manufacturing convenience and may include an opaque material as a light shield (claim 15) as consistent with the goal of improving yield as taught in Kaneko.

As to claim 16, it may be presumed that data lines and storage capacitor electrode are formed of the same material simultaneously for manufacturing convenience as taught in Kaneko.

As to claims 20 and 21, for directions in which the protrusion extends, please refer to Figure 1A.

As to claims 34-37 and 41-42, Applicant's recited steps of a method for fabricating a liquid crystal display device would have been rendered obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in light of the device as disclosed and taught in and by the above cited references.

Claims 17-19 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States patent 5,995,177 (to Fujikawa et al.) in view of United States Patent 6,091,473 (to Hebiguchi) in further view of United States Patent 6,587,162 B1 (to Kaneko et al.) and further in view of United States Patent 5,151,806 (to Kawamoto et al.).

As to claims 17-19, Fujikawa does not appear to explicitly specify a second capacitor electrode overlapping a portion of the gate line to form a second storage capacitor, first and second capacitor electrodes simultaneously formed of the same material, and pixel electrode electrically connected with the second capacitor electrode.

Kawamoto discloses a liquid crystal display apparatus having a series combination of the storage capacitors wherein, with reference to Figure 38, a floating electrode (12) overlapping a portion of the gate line (24) and a pixel electrode connected with first and second storage

electrodes (Kawamoto, claims 1-3) for formation of storage capacitance and to prevent short-circuiting (ABS, entire patent).

Kawamoto is evidence that ordinary workers in the field of liquid crystals would have had the reason, suggestion, and motivation to include a second capacitor electrode overlapping a portion of a gate line and connected to the pixel electrode to prevent short-circuiting and for storage capacitance.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to include the structure of Kawamoto into the array substrate of Fujikawa to prevent short-circuiting and for storage capacitance.

As to claims 38-40, Applicant's recited steps of a method for fabricating a liquid crystal display device would have been rendered obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in light of the device as disclosed and taught in and by the above cited references.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio
Patent Examiner
Art Unit 2871

JDG

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800